REMARKS

Claims 23, 25-37, and 41-47 are currently pending. Claims 23, 25-32, 34-37, 41, and 44 were allowed. Claims 33, 42, 43, and 45-47 were rejected. No amendments are made in this paper. For at least the following reasons, Applicant respectfully submits that each of the presently pending claims is in condition for allowance.

Allowed Claims

Claims 23, 25-32, 34-37, 41, and 44 were allowed. Applicant thanks the Examiner for his work on this matter.

Rejection to Claim 47 under 35 U.S.C. §112

Claim 47 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses the rejection.

The Office Action states that Claim 47 is indefinite because it is not clear what are the "first gate-to-source voltage", "another node", "a second gate-to-source voltage" and "to provide a voltage drop between the other node and the input node". The Office Action also states that it is not clear how the "voltage drop" is provided between the control input node and another node; and between the other node and the input node.

In one embodiment, the claim language is applicable as follows. In circuit 800 of Applicant's FIG. 8, the first gate-to-source voltage is the gate-to-source voltage of transistor 830, the second gate-to-source voltage is the gate-to-source voltage of transistor 840, recited "input node" is the node to which transistor 610, the gate of transistor 840, and V_{IN} are all coupled; recited "other node" is the node to which the drain of transistor 830, the gate of transistor 830, and the source of transistor 840 are all coupled; and recited "control input node" is the node to which the

gate of transistor 610, the source of transistor 830, and current source 850 are all coupled. In operation, circuit 800 employs the gate-to-source voltage of transistor 830 to provide a voltage drop between the control input node (to which the gate of transistor 610 is coupled) and the other node. Further, circuit 800 employs the gate-to-source voltage of transistor 840 to provide a voltage drop between the other node and the input node (at which voltage V_{IN} is received). The gate-to-source voltage of transistor 830 and transistor 840 are both provided based on the received bias current. It is understood that the scope of Claim 47 is not limited in any way to the circuit of FIG. 8 discussed above, which is described by way of illustration and example only.

Applicants also note an unusual aspect of the use of the word "other" in the English language. The English language is subject to many exceptions to usual rules. For example, one might expect that the plural of the word "moose" would be "mooses", but in fact, the plural of the word "moose" is simply "moose". Moose is a word in the English language to which the normal rules of forming a plural do not apply. Similarly, the rules to which articles such as "an" and "the" are applied to the word "other" is subject to an exception to the standard rules. For example, one would not state, "the system includes: a circuit and an other circuit, wherein the other circuit is coupled to the circuit." This would be grammatically incorrect. Instead, the word "another" is used where one might ordinarily expect to say "an other". The words "an" and "other" are basically combined into one word, "another". Accordingly, the above sentence would be stated, "the system includes: a circuit and another circuit, wherein the other circuit is coupled to the circuit." Note that in this example, "another circuit" (i.e. an other circuit) gives antecedent basis for "other circuit". It would also be grammatically incorrect to write the sentence as, "the system includes: a circuit and another circuit, wherein the another circuit is coupled to the circuit", because "the another circuit" would basically mean "the an other circuit", which makes no sense.

Claims 33 and 42

Claims 33 and 42 were rejected under 35 U.S.C. §102(b) as being anticipated by Li et al. (U.S. Patent No. 6,373,324, hereinafter Li).

The rejection to Claim 33 is respectfully traversed, at least because Li does not disclose, "provide a control input voltage at the control input node such that a voltage difference between the control input voltage and an input voltage at the input node is substantially constant **during an on condition of the first transmission gate**" (emphasis added). In Fig. 3 of Li, transistors 313 and 314 are both back-biased when switch 312 is on. At Col 5, lines 6-19, Li states that, when clock 34 is high and clock 31 is low, transistor 313 is turned on, and switching transistor 312 is off but it is nearly turned on. When transistor 313 is turned on, switching transistor 312 is off. Further, Li states that transistor 314 serves to ensure that the switching transistor 312 is turned off in order to prevent back flow from node 3N2 to node 3N1. Transistor 314 is specifically used to **ensure** that transistor 312 is off. When transistor 314 is on, switching transistor 312 is off. Accordingly, neither transistor 313 nor transistor 314 provides a substantially constant voltage difference during the on condition of the transmission gate.

The rejection to Claim 42 is respectfully traversed at least for reasons analogous to those stated above with regard to Claim 33.

Claims 43 and 45-47

Claims 43 and 45-47 were rejected under 35 U.S.C. §102(b) as being anticipated by Singer et al. (U.S. Patent No. 6,118,326, hereinafter Singer).

The rejection to Claim 43 is respectfully traversed. Claim 43 is respectfully submitted to be allowable at least because Singer does not disclose, "the boost voltage is greater than the supply voltage even if an input voltage at the input node is zero", in conjunction with the other elements of Applicant's Claim 43. In its rejection, the Office Action uses the voltage at node N1 of FIG. 7 of Singer as the supposed "boost voltage", and uses S4 of FIG. 7 of Singer as the supposed "current source" that is coupled between node N1 (the supposed boost node) and node N3 (the control input node). In circuit shown in FIG. 7 of Singer, during Interval 2, the voltage at node N1 is Vin+V++-V--. See Column 12, line 30 of Singer. Accordingly, in the circuit shown in FIG. 7 of Singer, during Interval 2, if Vin is zero volts, the voltage at node N1 is equal to the supply voltage V++,

rather than being greater than the supply voltage. Also, during Interval 1, the voltage at node N1 is simply V++, rather than being greater than the supply voltage.

The rejection to Claim 45 is respectfully traversed. It is respectfully submitted that the circuit of FIG. 7 of Signer does not disclose, "the current source circuit, the first component, and the second component are coupled in series." The Office Action states, "Current source circuit (S4) and first, second components (S1, S7) are connected in series." Applicants respectfully disagree. It is readily apparent from inspection of FIG. 7 of Singer that S1, S4, and S7 are not connected in series. S1 is not connected in series with S4, S4 is not connected in series with S7, and S1 is not connected in series with S7.

The rejection to Claim 46 is respectfully traversed. It is respectfully submitted that the circuit of FIG. 7 of Signer does not disclose, "maintaining the substantially constant voltage difference between the control input voltage and the input voltage is not accomplished via capacitive sampling", as recited in Applicant's Claim 46.

In the circuit of FIG. 7 of Singer, during Interval 1, transistor M1 is off, and a voltage of [(V++)-(V--)] is sampled across capacitor Cboot. During Interval 2, transistor M1 is on, capacitor Cboot is placed in parallel with the gate-to-source voltage of transistor M1. Since a voltage of [(V++)-(V--)] is sampled across capacitor during Interval 1, during Interval 2, capacitor Cboot causes the gate-to-source voltage to be approximately maintained at about [(V++)-(V--)]. Accordingly, when transistor M1 is on, the circuit of FIG. 7 of Singer causes the difference between the input voltage and the control input voltage to be maintained to a substantially constant voltage via capacitive sampling. Accordingly, the circuit of FIG. 7 of Singer does not meet the limitation, "maintaining the substantially constant voltage difference between the control input voltage and the input voltage is not accomplished via capacitive sampling", as recited in Applicant's Claim 46.

The rejection to Claim 47 under 35 U.S.C. § 102 is respectfully traversed. It is respectfully submitted that the circuit of FIG. 7 of Signer does not disclose, "providing the control input signal includes: receiving the bias current at a control input node, wherein the control input of the switch circuit is coupled to the control input node; employing a first gate-to-source voltage to provide a

voltage drop between the control input node and another node; and employing a second gate-to-source voltage to provide a voltage drop between the other node and the input node", as recited in Applicant's Claim 47.

As discussed above, during Interval 2, the circuit of FIG. 7 of Singer uses capacitor Cboot to provide a voltage drop between node N3 and voltage Vin. The circuit of FIG. 7 of Singer does not employ two gate-to-source voltages to provide a voltage drop between node N3 and voltage Vin. Accordingly, the circuit of FIG. 7 of Singer does not disclose, "providing the control input signal includes: receiving the bias current at a control input node, wherein the control input of the switch circuit is coupled to the control input node; employing a first gate-to-source voltage to provide a voltage drop between the control input node and another node; and employing a second gate-to-source voltage to provide a voltage drop between the other node and the input node", as recited in Applicant's Claim 47."

Claims 43 and 45-47 are respectfully submitted to be allowable for at least the reasons stated above, and notice to that effect is earnestly solicited.

CONCLUSION

It is respectfully submitted that each of the presently pending claims (Claims 23, 25-37, and 41-47) are in condition for allowance and notification to that effect is requested. Examiner is invited to contact the Applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

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